UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,287,208 B2
APPLICATION NO. : 10/814449
DATED : October 23, 2007
INVENTOR(S) : Dybsetter et al.

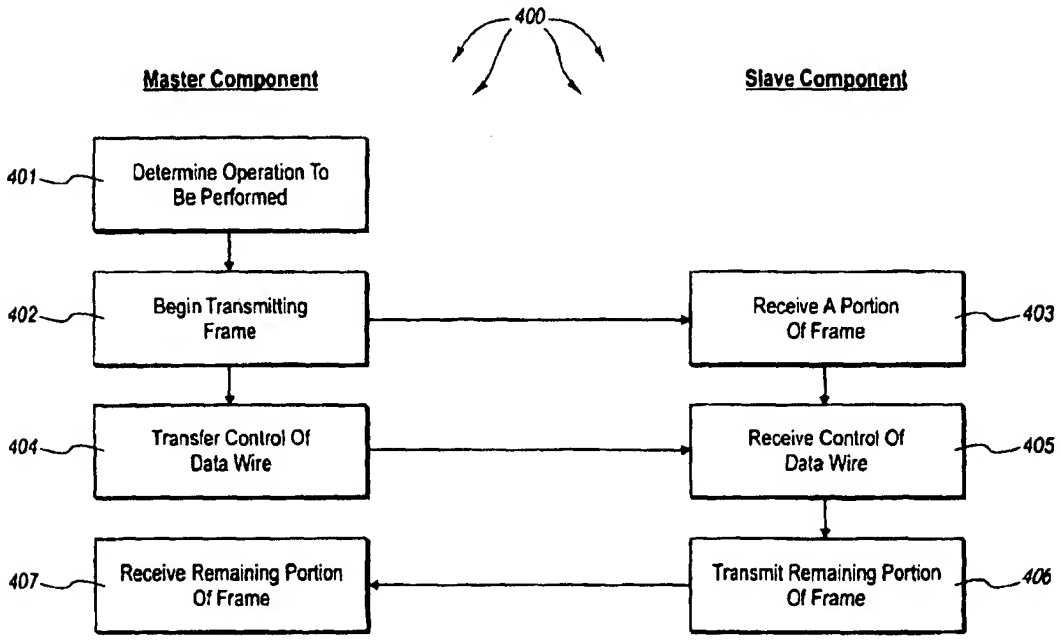
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page

Delete Title Page showing an illustrative figure, and substitute the attached Title Page therefor.

Drawings

Sheet 5, replace Figure 4 with the figure depicted herein below, wherein the second instance of "405" referring to "Transmit Remaining Portion of Frame" has been changed to --406--



Signed and Sealed this

Twenty-first Day of December, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

Drawings
Sheet 7, replace Figure 7 with the figure depicted herein below, wherein under the "Bits" column: "28:26" has been changed to --28:24--, "25:19" has been changed to --23:19--, "16:1" has been changed to --16:01--, and "0" has been changed to --00--

```
-------------------------------------------------------
          PRE   ST OP PRT   DEV   TA ADDRESS/DATA     IDLE
          6   3 33 32 2   2 2   1 11 1              0 0
          4   3 21 09 8   4 3   9 87 6              1 0
--------- ----- -- -- ----- ----- -- ---------------- -
Address   1...1 00 00 PPPPP EEEEE 10 AAAAAAAAAAAAAAAA Z
Write     1...1 00 01 PPPPP EEEEE 10 DDDDDDDDDDDDDDDD Z
Read      1...1 00 11 PPPPP EEEEE Z0 DDDDDDDDDDDDDDDD Z
Read inc. 1...1 00 10 PPPPP EEEEE Z0 DDDDDDDDDDDDDDDD Z
--------- ----- -- -- ----- ----- -- ---------------- -

Field     Bits
-------   -----
PRE       64:33 (32) -- preamble
ST        32:31  (2) -- start of frame
OP        30:29  (2) -- operation code
(ADDR=00,WR=01,RD=11,RDINC=10)
PRTAD     28:24  (5) -- port address
DEVAD     23:19  (5) -- device address
TA        18:17  (2) -- bus turnaround phase & transfer acknowledge
ADDR/DATA 16:01 (16) -- address or data
IDLE          00  (1) -- end of transmission
                ----
                 65  -- transaction bit length
```

Fig. 7
(Prior Art)

Column 2
Line 18, change "as that the" to --as the--
Line 27, change "have" to --having--

Column 3
Line 6, change "component is" to --component that is--

Column 5
Line 7, change "components" to --component--
Line 24, change "and" to --an--

Column 6
Line 41, change "none-preamble" to --non-preamble--

Column 7
Line 10, change "with rest" to --with the rest--

Column 8
Line 59, change "represented" to --represent--
Line 63, change "more further" to --further--

Column 9
Line 25, change "none" to --neither--
Line 38, change "given" to --giving--

Column 10
Line 34, change "communications" to --communication--

Column 11
Line 23, change "bus" to --wire--
Line 24, change "bus" to --wire--
Line 46, change "are absence" to --are absent--

Column 12
Line 9, change "referred" to --referring--
Line 45, change "bit rates transfers" to --bit rate transfers--

Column 13
Line 26, change "signal" to --line--
Line 51, change "16bit" to --16-bit--
Line 61, change "control" to --controller--

Column 14
Line 4, change "being" to --is--

Column 15
Claim 11, line 52, change "indication" to --indicating--
Claim 11, line 55, change "component;" to --component; and--

Column 17
Claim 19, line 3, change "that indicative" to --indicative--
Claim 25, line 25, change "slave component" to --master component--
Claim 25, line 36, change "that indicative" to --indicative--

Column 18
Claim 31, line 12, change "that indicative" to --indicative--
Claim 31, line 22, change "that indicative" to --indicative--
Claim 39, line 45, change "38" to --37--
Claim 40, line 48, change "38" to --37--
Claim 41, line 51, change "38" to --37--
Claim 42, line 54, change "38" to --37--
Claim 43, line 57, change "38" to --37--
Claim 44, line 60, change "38" to --37--
Claim 45, line 63, change "38" to --37--

(12) **United States Patent**
Dybsetter et al.

(10) **Patent No.: US 7,287,208 B2**
(45) **Date of Patent: Oct. 23, 2007**

(54) **TWO-WIRE INTERFACE HAVING EMBEDDED PER FRAME RELIABILITY INFORMATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 742 days.

(21) Appl. No.: **10/814,449**

(22) Filed: **Mar. 31, 2004**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Provisional application No. 60/529,918, filed on Dec. 15, 2003.

(51) **Int. Cl.**
H03M 13/00 (2006.01)

(52) **U.S. Cl.** **714/758**

(58) **Field of Classification Search** 714/758
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,571,346 B1 * 5/2003 Dreps et al. 713/600

OTHER PUBLICATIONS

U.S. Appl. No. 10/814,483, filed Mar. 31, 2004, Dybsetter et al.

* cited by examiner

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(57) **ABSTRACT**

A guaranteed two-wire interface in which upon determining that an operation is to be performed on a slave component, the master component begins transmitting the frame to the slave component including an identification of the operation to be performed. The master component then transfers control of the data wire to the slave component. The slave component then transmits a remaining portion of the frame to the master component over the data wire. The frame includes reliability information such as cyclic redundancy checking data or acknowledgement data that the master component may then use to determine whether the operation was successful.

45 Claims, 7 Drawing Sheets